FIG.1

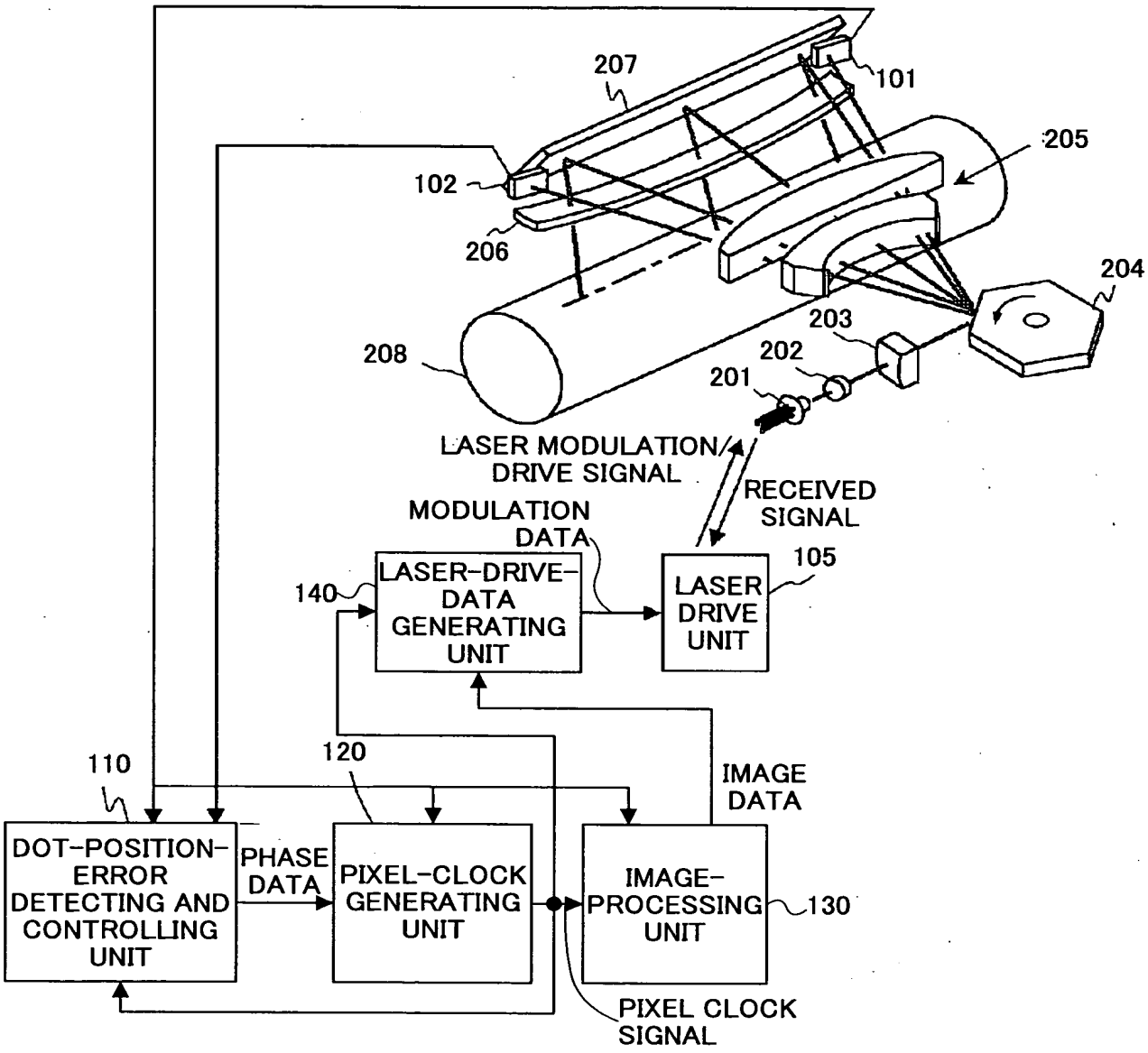

207
101
205
102
206
204
203
208
202
201
LASER MODULATION/
DRIVE SIGNAL
RECEIVED
SIGNAL
MODULATION
DATA
140
LASER-DRIVE-
DATA
GENERATING
UNIT
LASER
DRIVE
UNIT
105
110
120
IMAGE
DATA
DOT-POSITION-
ERROR
DETECTING AND
CONTROLLING
UNIT
PHASE
DATA
PIXEL-CLOCK
GENERATING
UNIT
IMAGE-
PROCESSING
UNIT
130
PIXEL CLOCK
SIGNAL

FIG.2

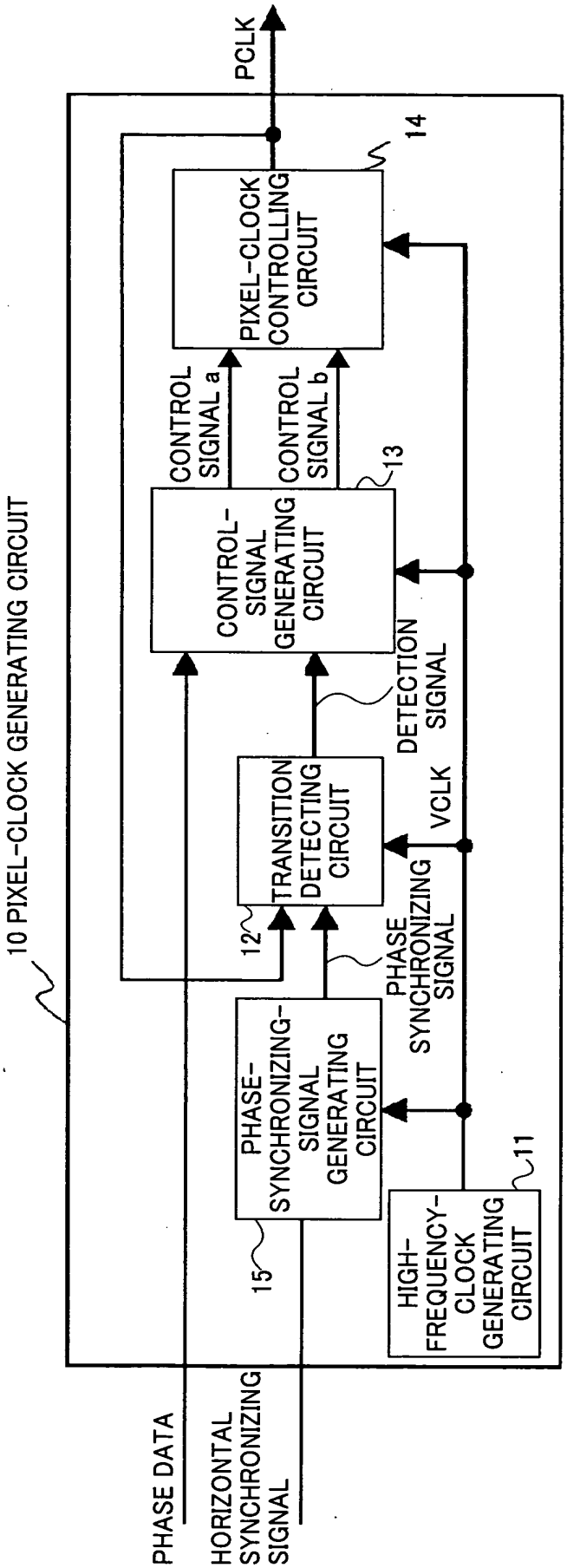

10 PIXEL-CLOCK GENERATING CIRCUIT
PCLK
14
PIXEL-CLOCK CONTROLLING CIRCUIT
CONTROL SIGNAL a
CONTROL SIGNAL b
13
CONTROL-SIGNAL GENERATING CIRCUIT
DETECTION SIGNAL
12
TRANSITION DETECTING CIRCUIT
VCLK
PHASE SYNCHRONIZING SIGNAL
15
PHASE-SYNCHRONIZING-SIGNAL GENERATING CIRCUIT
11
HIGH-FREQUENCY-CLOCK GENERATING CIRCUIT
PHASE DATA
HORIZONTAL SYNCHRONIZING SIGNAL

FIG.3

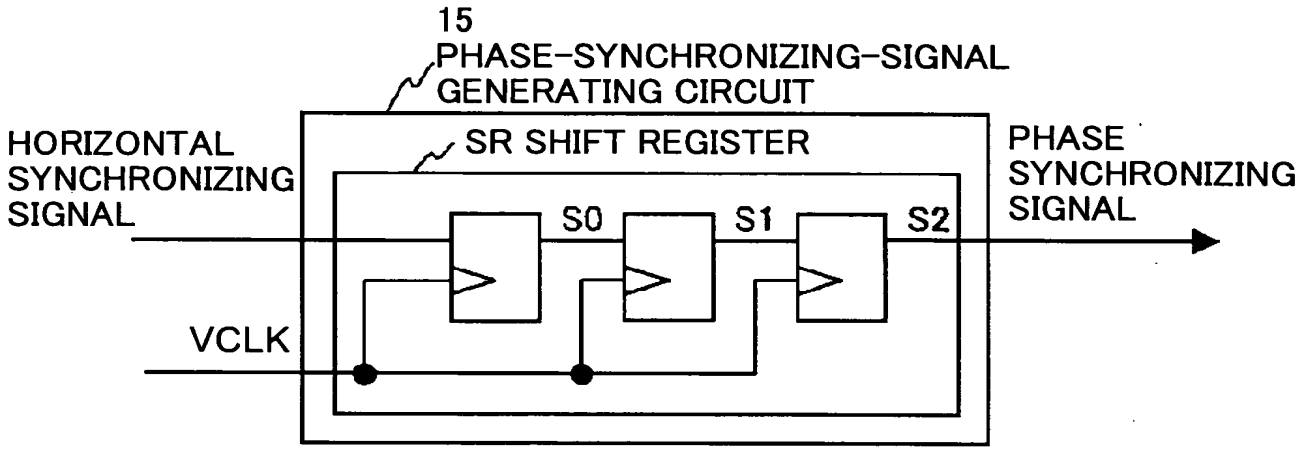

15
PHASE-SYNCHRONIZING-SIGNAL
GENERATING CIRCUIT
SR SHIFT REGISTER
HORIZONTAL
SYNCHRONIZING
SIGNAL
VCLK
S0
S1
S2
PHASE
SYNCHRONIZING
SIGNAL

FIG.4

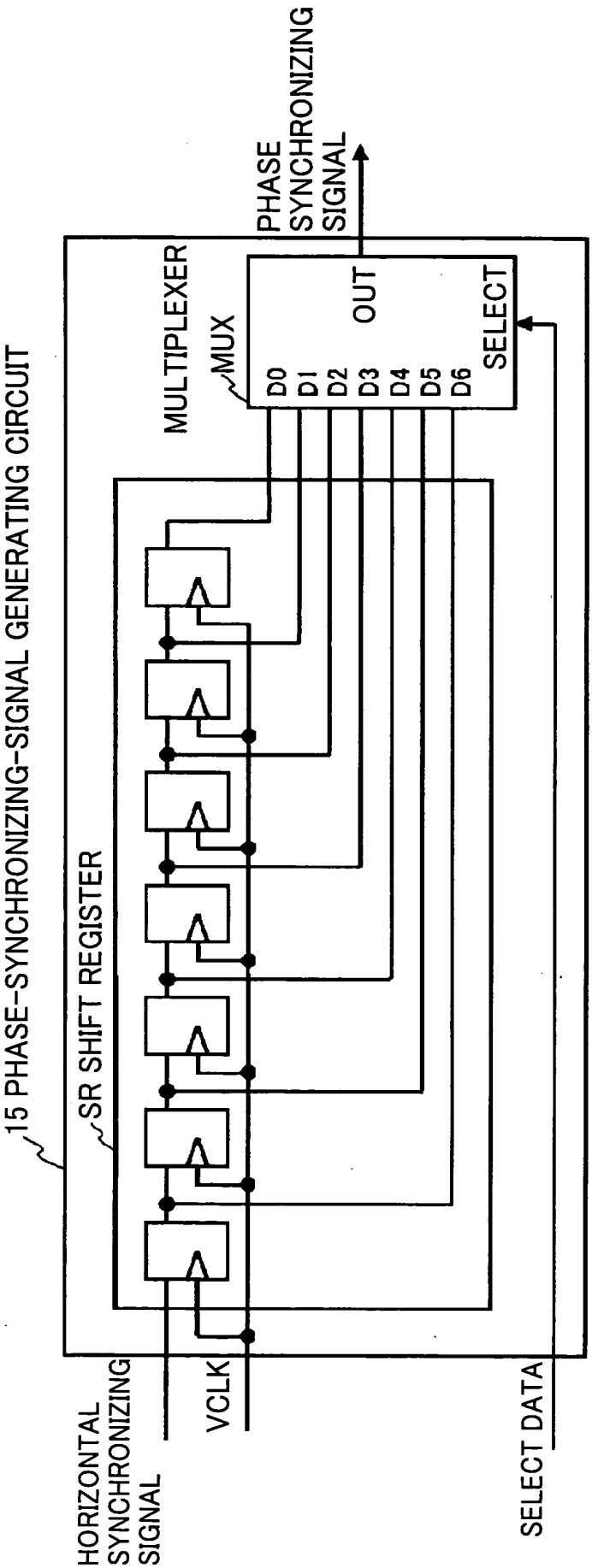

15 PHASE-SYNCHRONIZING-SIGNAL GENERATING CIRCUIT
SR SHIFT REGISTER
MULTIPLEXER
MUX
D0
D1
D2
D3
D4
D5
D6
OUT
SELECT
PHASE SYNCHRONIZING SIGNAL
HORIZONTAL SYNCHRONIZING SIGNAL
VCLK
SELECT DATA

FIG.5

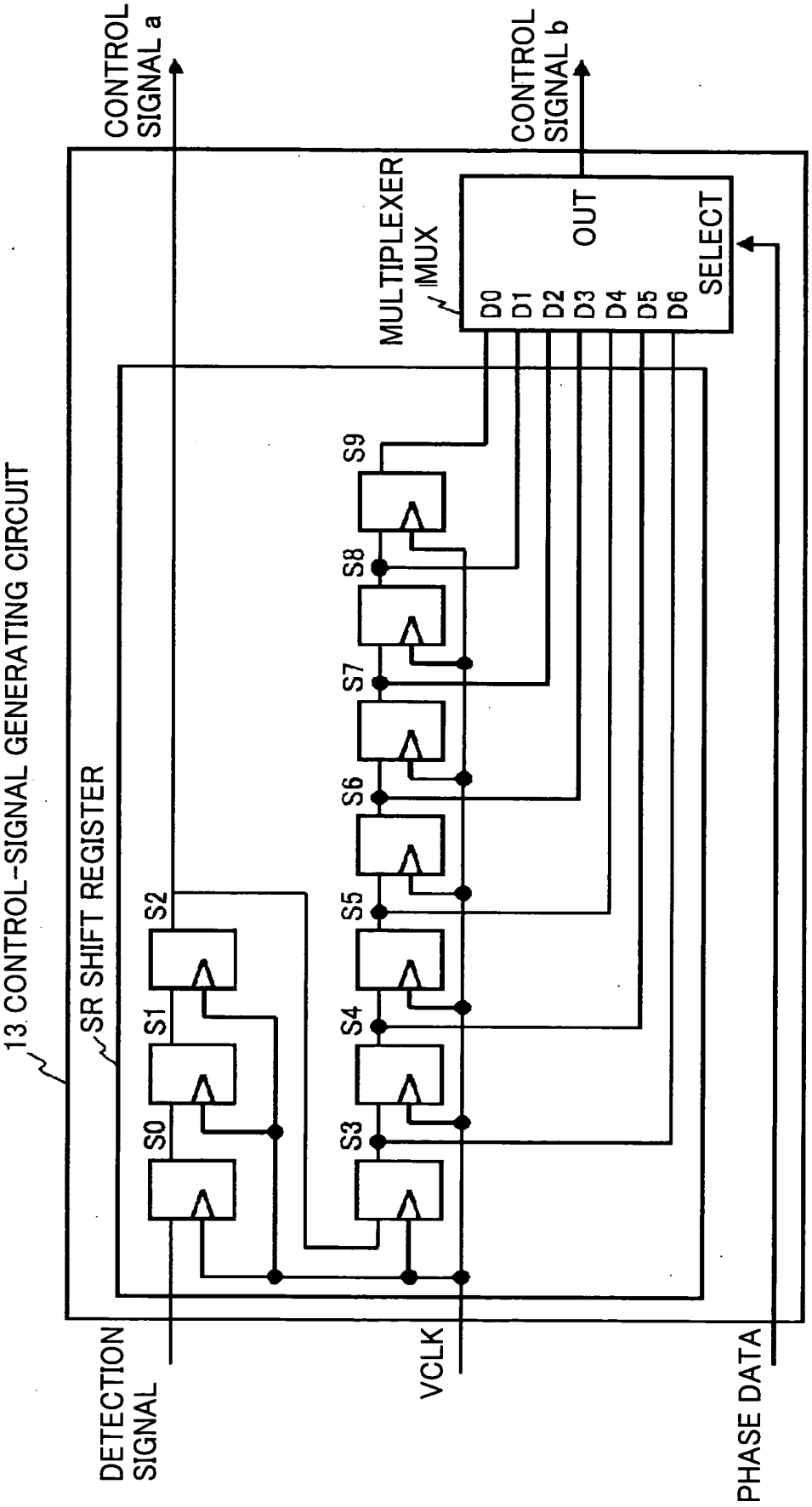

13 CONTROL-SIGNAL GENERATING CIRCUIT
SR SHIFT REGISTER
S0
S1
S2
S3
S4
S5
S6
S7
S8
S9
MULTIPLEXER MUX
D0
D1
D2
D3
D4
D5
D6
OUT
SELECT
CONTROL SIGNAL a
CONTROL SIGNAL b
DETECTION SIGNAL
VCLK
PHASE DATA

FIG.6

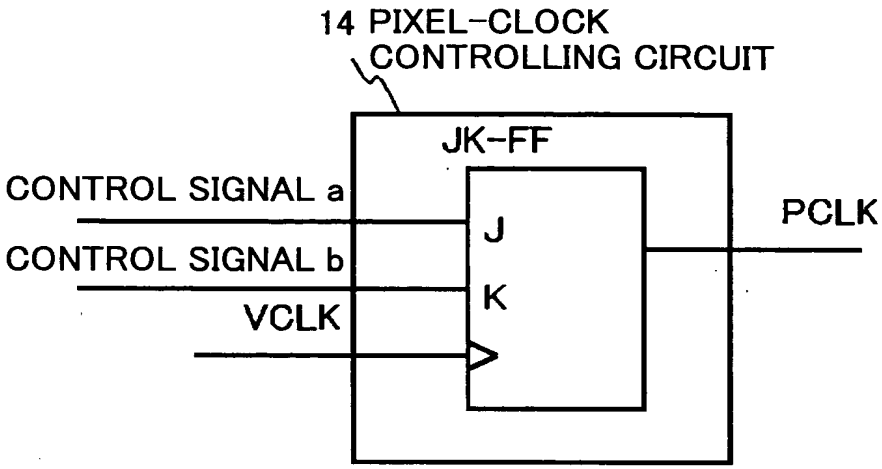

14 PIXEL-CLOCK
CONTROLLING CIRCUIT
JK-FF
CONTROL SIGNAL a
CONTROL SIGNAL b
VCLK
J
K
PCLK

FIG.7

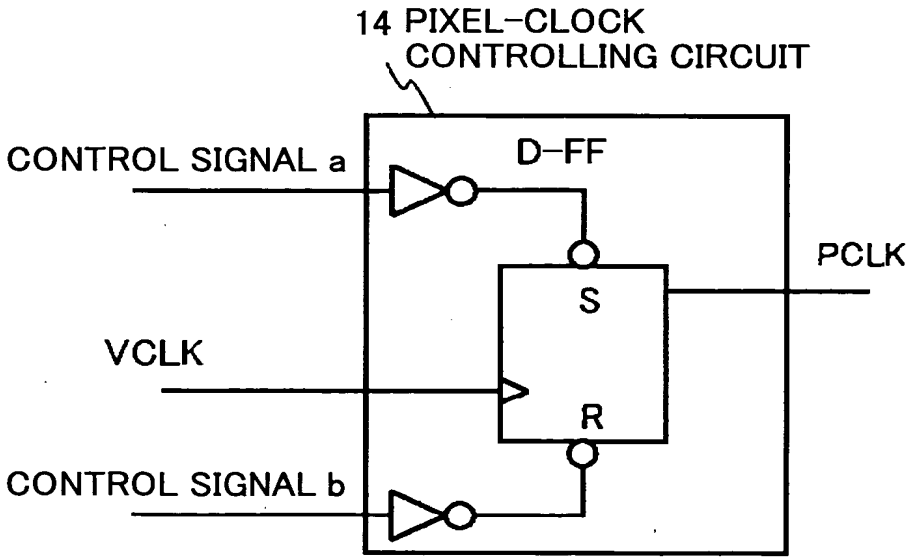

14 PIXEL-CLOCK
CONTROLLING CIRCUIT
D-FF
CONTROL SIGNAL a
VCLK
CONTROL SIGNAL b
S
R
PCLK

FIG.8A

PHASE SHIFT AMOUNT	PHASE DATA 3bit
3/8 PCLK DELAY	000
2/8 PCLK DELAY	001
1/8 PCLK DELAY	010
0	011
1/8 PCLK ADVANCEMENT	100
2/8 PCLK ADVANCEMENT	101
3/8 PCLK ADVANCEMENT	110

FIG.8B

PHASE DATA 3bit	OUT
000	D0
001	D1
010	D2
011	D3
100	D4
101	D5
110	D6

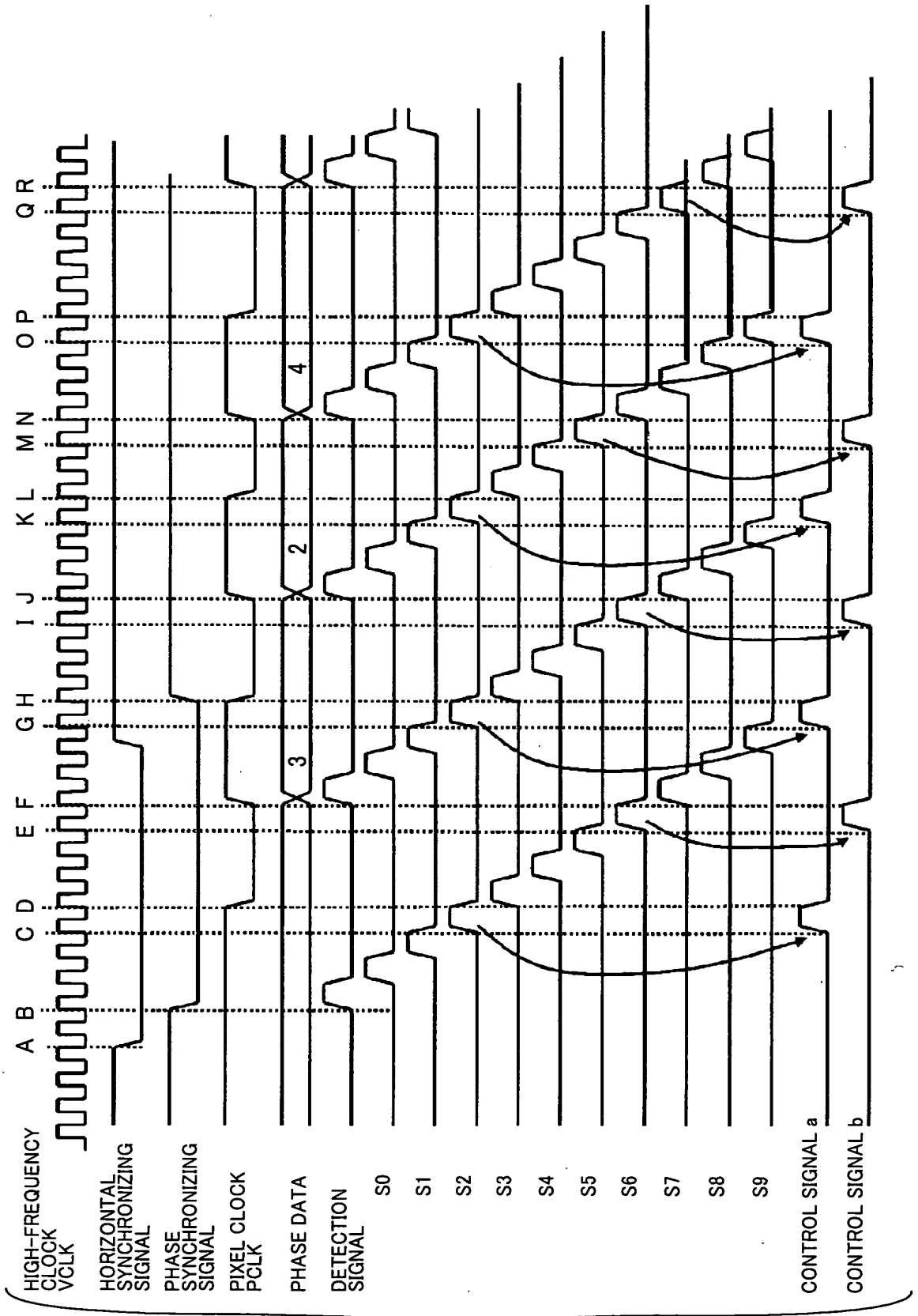

PHASE SHIFT AMOUNT 0
PHASE SHIFT AMOUNT -1
PHASE SHIFT AMOUNT +1
A B C D E F G H I J K L M N O P Q R
HIGH-FREQUENCY CLOCK VCLK
HORIZONTAL SYNCHRONIZING SIGNAL
PHASE SYNCHRONIZING SIGNAL
PIXEL CLOCK PCLK
PHASE DATA
DETECTION SIGNAL
S0
S1
S2
S3
S4
S5
S6
S7
S8
S9
CONTROL SIGNAL a
CONTROL SIGNAL b
2
3
4

FIG.9

FIG.10

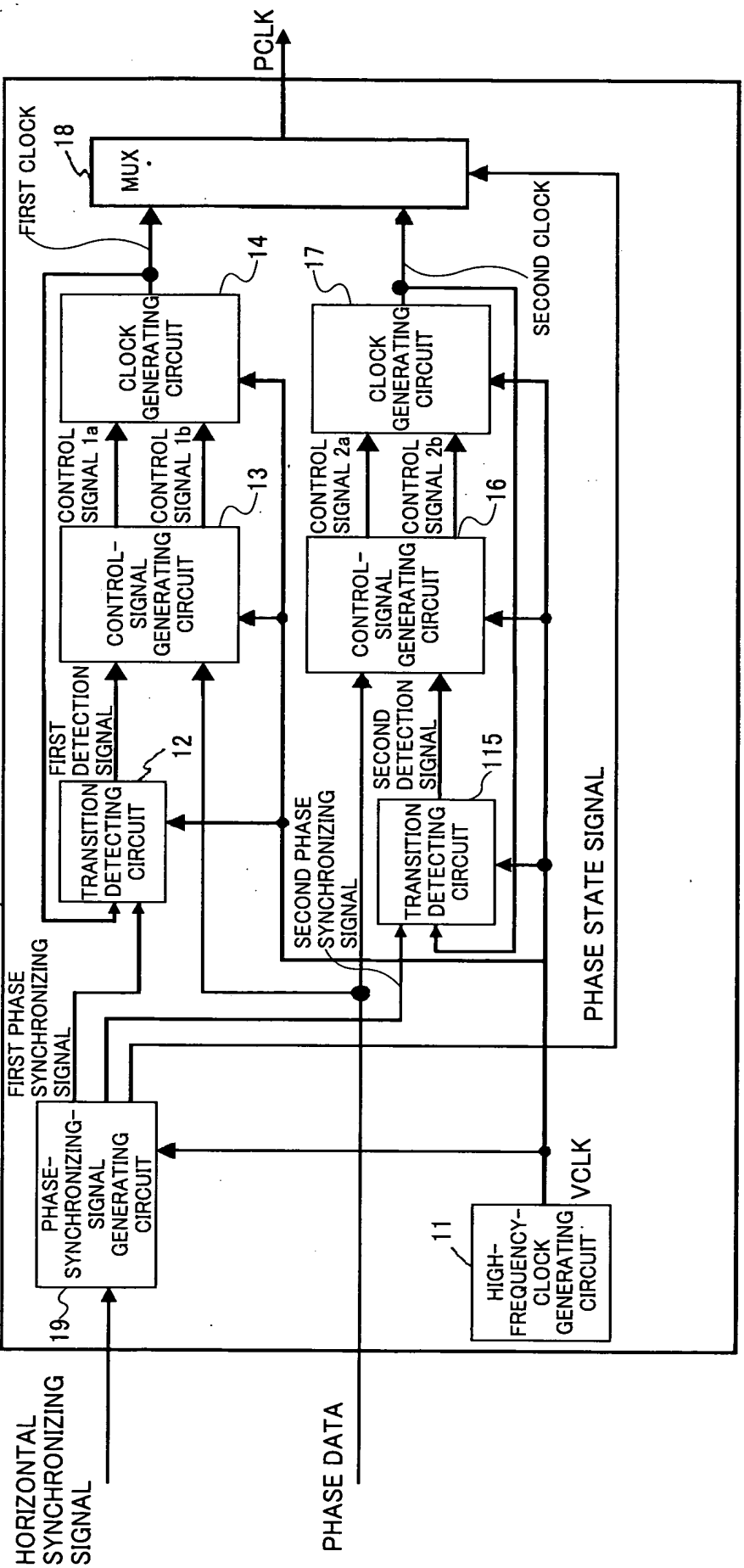
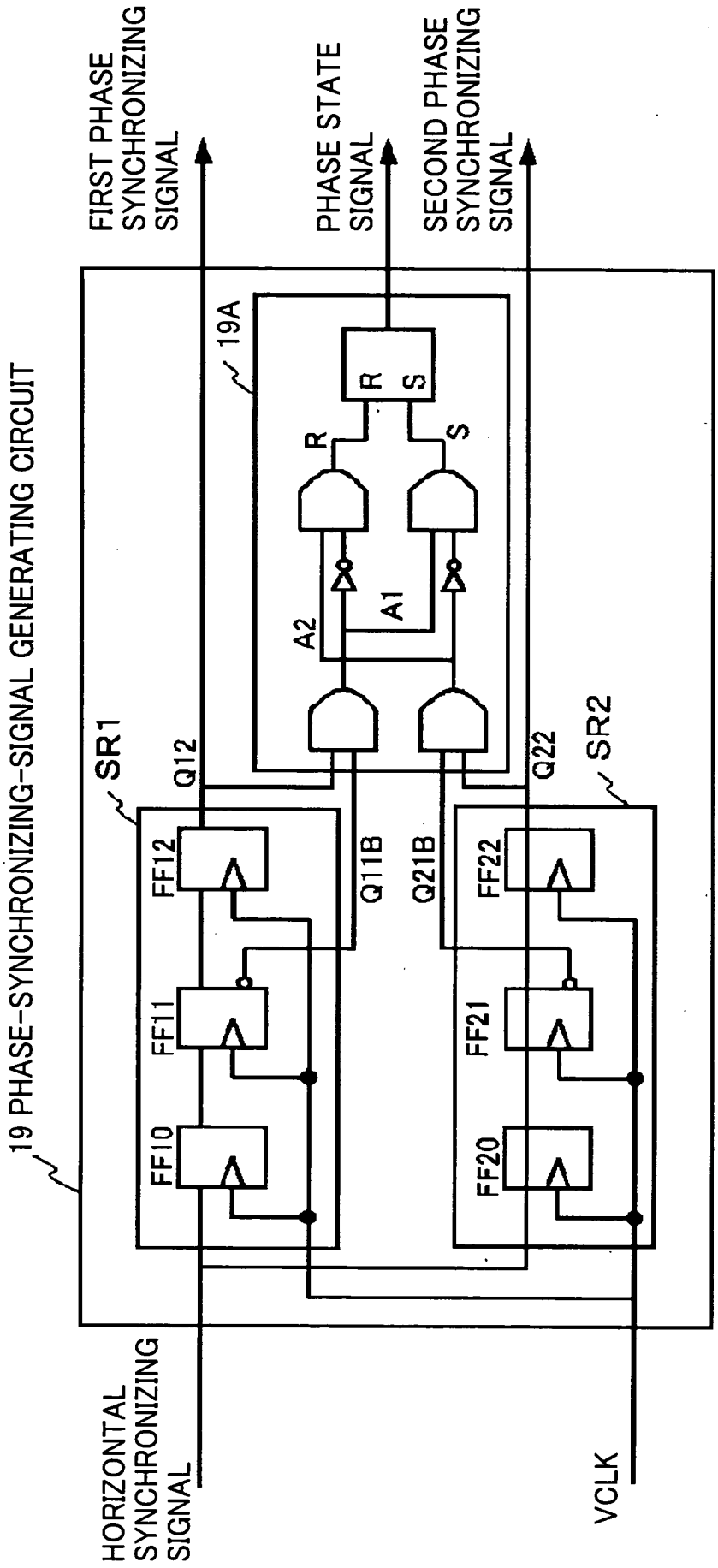

10 PIXEL-CLOCK GENERATING CIRCUIT
PCLK
MUX
18
FIRST CLOCK
SECOND CLOCK
CLOCK GENERATING CIRCUIT
14
17
CONTROL SIGNAL 1a
CONTROL SIGNAL 1b
CONTROL SIGNAL 2a
CONTROL SIGNAL 2b
CONTROL-SIGNAL GENERATING CIRCUIT
13
16
FIRST DETECTION SIGNAL
SECOND DETECTION SIGNAL
TRANSITION DETECTING CIRCUIT
12
115
FIRST PHASE SYNCHRONIZING SIGNAL
SECOND PHASE SYNCHRONIZING SIGNAL
PHASE STATE SIGNAL
PHASE-SYNCHRONIZING-SIGNAL GENERATING CIRCUIT
19
HIGH-FREQUENCY-CLOCK GENERATING CIRCUIT
11
VCLK
HORIZONTAL SYNCHRONIZING SIGNAL
PHASE DATA

FIG.11


19 PHASE-SYNCHRONIZING-SIGNAL GENERATING CIRCUIT
FIRST PHASE SYNCHRONIZING SIGNAL
PHASE STATE SIGNAL
SECOND PHASE SYNCHRONIZING SIGNAL
19A
R
S
A2
A1
SR1
SR2
Q12
Q11B
Q21B
Q22
FF10
FF11
FF12
FF20
FF21
FF22
HORIZONTAL SYNCHRONIZING SIGNAL
VCLK

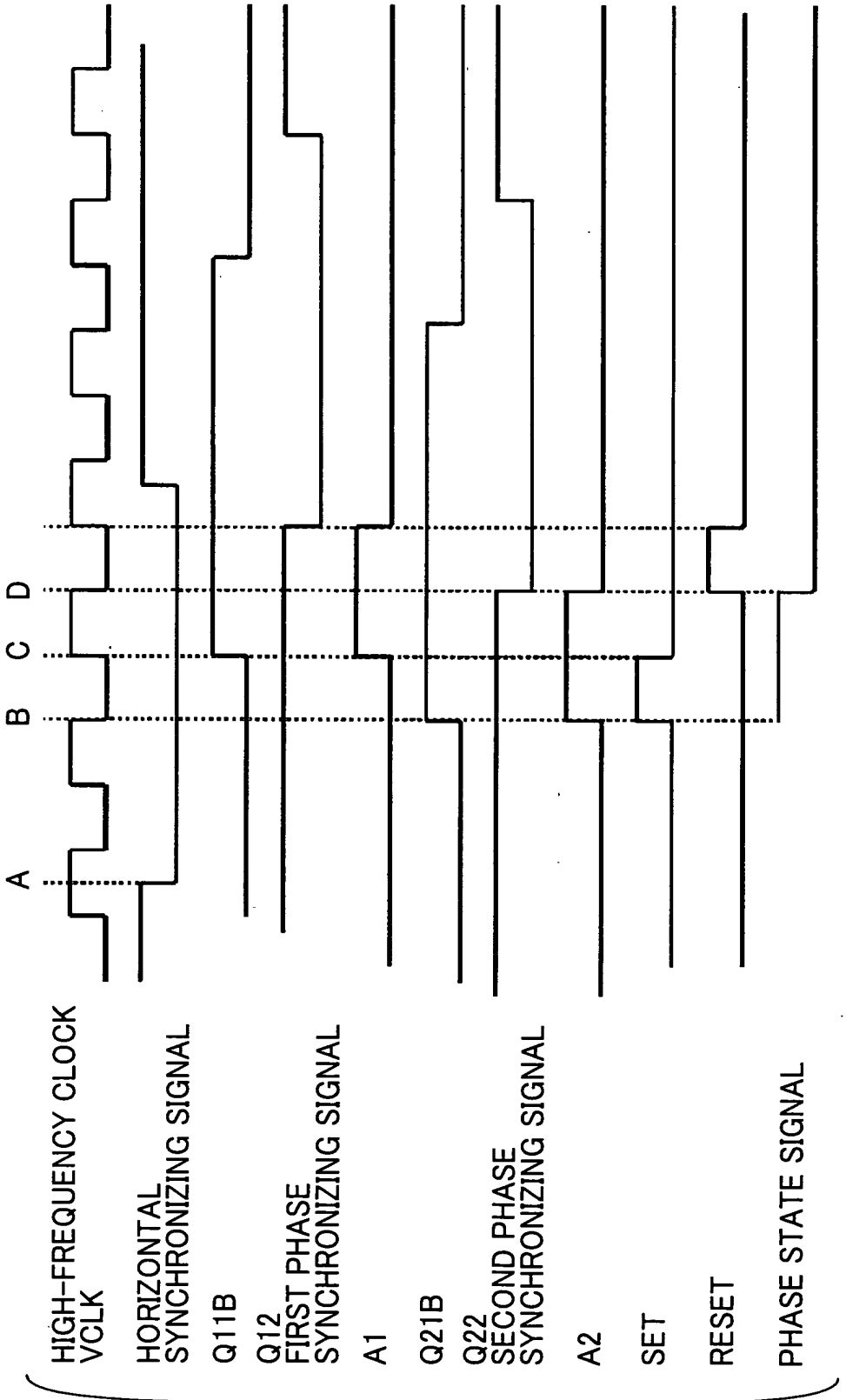

A
B
C
D
HIGH-FREQUENCY CLOCK VCLK
HORIZONTAL SYNCHRONIZING SIGNAL
Q11B
Q12
FIRST PHASE SYNCHRONIZING SIGNAL
A1
Q21B
Q22
SECOND PHASE SYNCHRONIZING SIGNAL
A2
SET
RESET
PHASE STATE SIGNAL

FIG.12

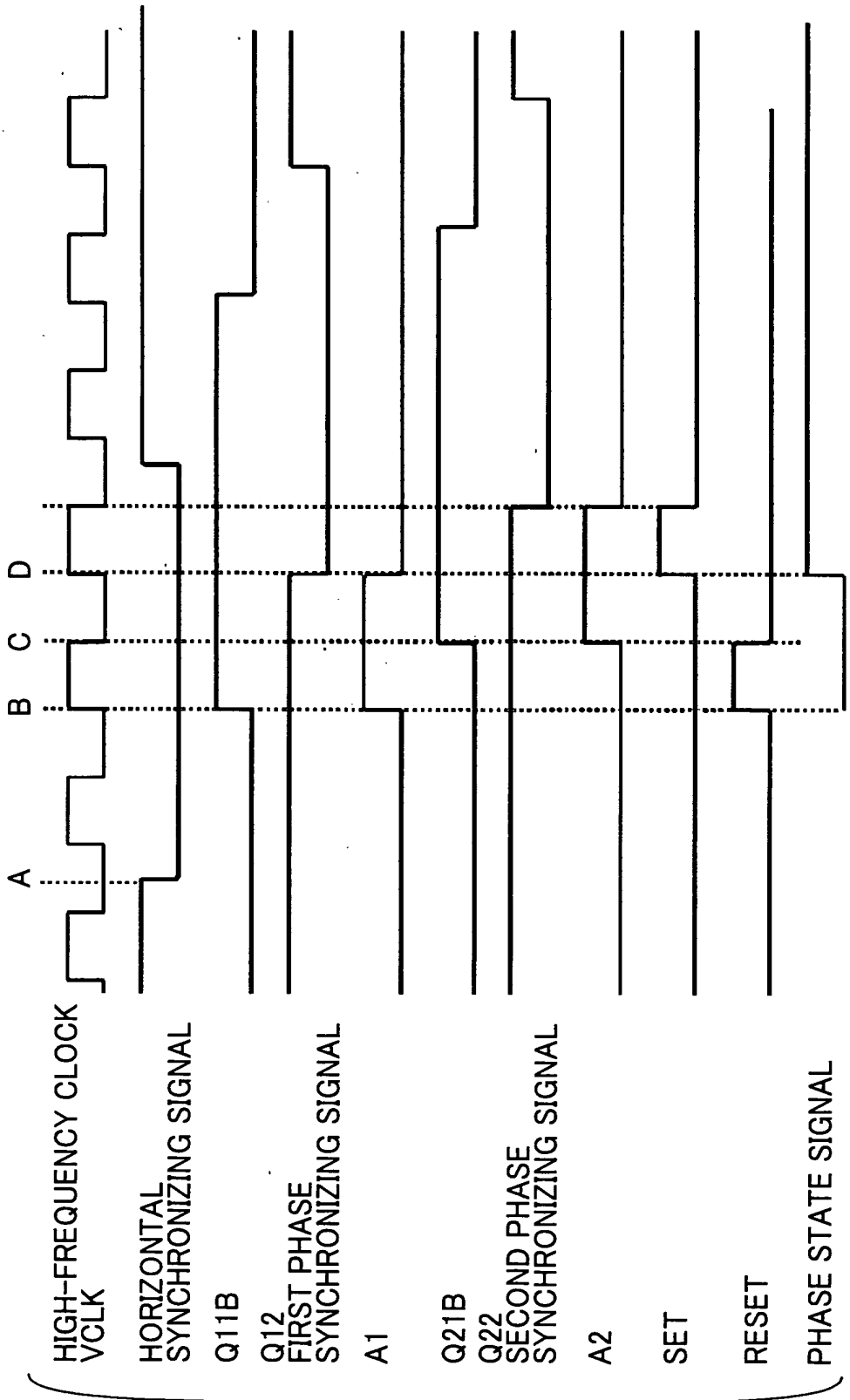
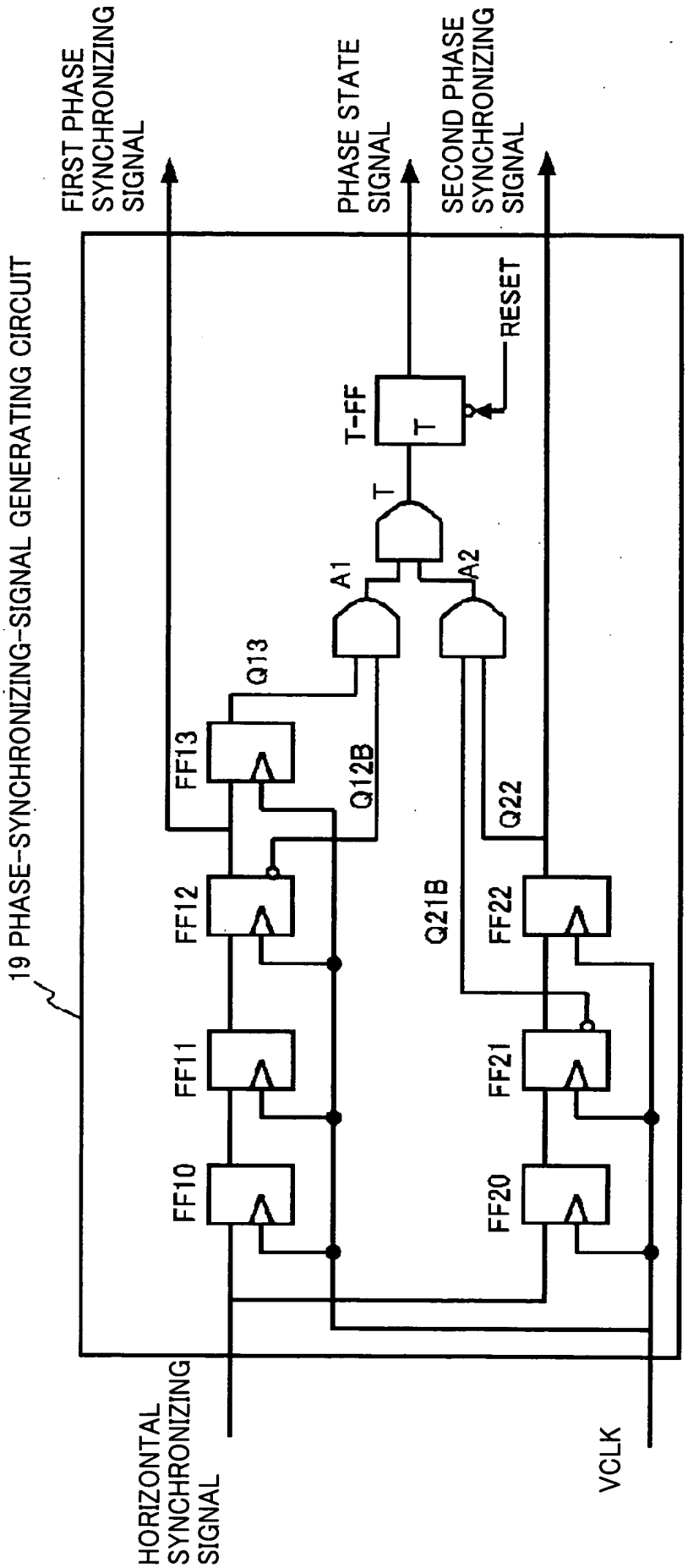

A
B
C
D
HIGH-FREQUENCY CLOCK VCLK
HORIZONTAL SYNCHRONIZING SIGNAL
Q11B
Q12
FIRST PHASE SYNCHRONIZING SIGNAL
A1
Q21B
Q22
SECOND PHASE SYNCHRONIZING SIGNAL
A2
SET
RESET
PHASE STATE SIGNAL

FIG.13

FIG.14


19 PHASE-SYNCHRONIZING-SIGNAL GENERATING CIRCUIT
FIRST PHASE SYNCHRONIZING SIGNAL
PHASE STATE SIGNAL
SECOND PHASE SYNCHRONIZING SIGNAL
RESET
T-FF
T
T
A1
A2
Q13
Q12B
Q21B
Q22
FF13
FF12
FF11
FF10
FF22
FF21
FF20
HORIZONTAL SYNCHRONIZING SIGNAL
VCLK

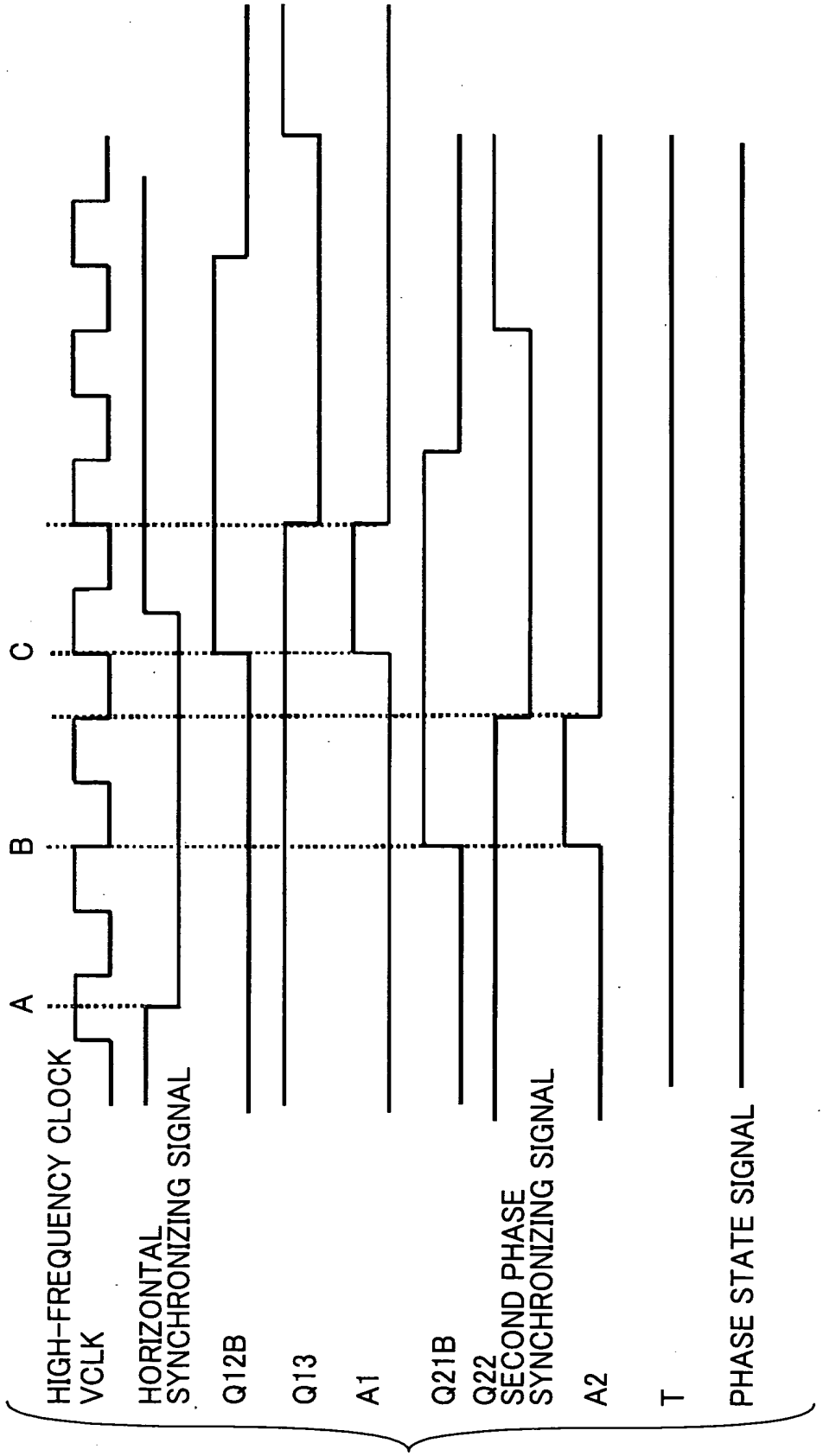

A
B
C
HIGH-FREQUENCY CLOCK VCLK
HORIZONTAL SYNCHRONIZING SIGNAL
Q12B
Q13
A1
Q21B
Q22
SECOND PHASE SYNCHRONIZING SIGNAL
A2
T
PHASE STATE SIGNAL

FIG.15

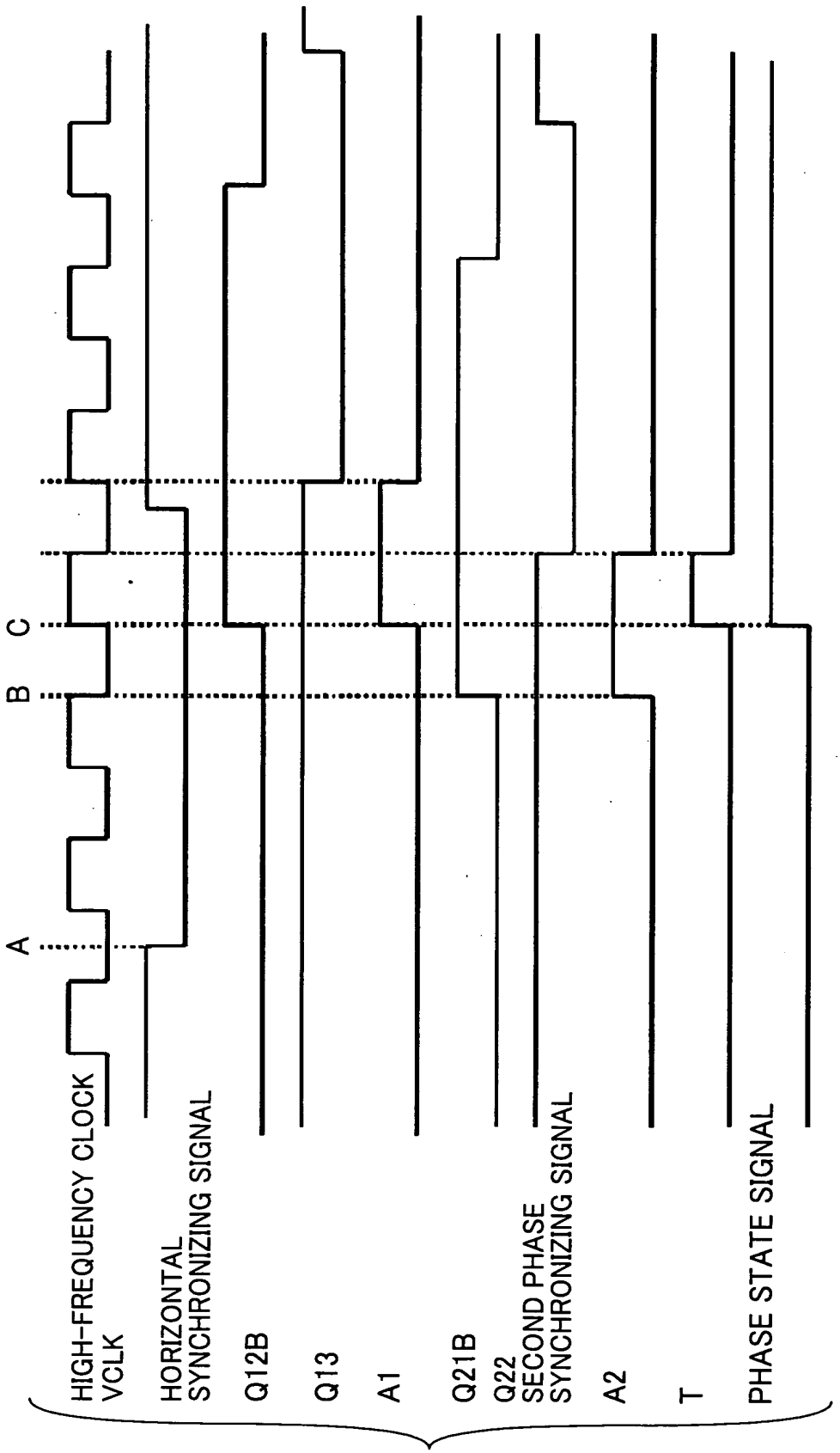

A
B
C
HIGH-FREQUENCY CLOCK VCLK
HORIZONTAL SYNCHRONIZING SIGNAL
Q12B
Q13
A1
Q21B
Q22
SECOND PHASE SYNCHRONIZING SIGNAL
A2
T
PHASE STATE SIGNAL

FIG.16

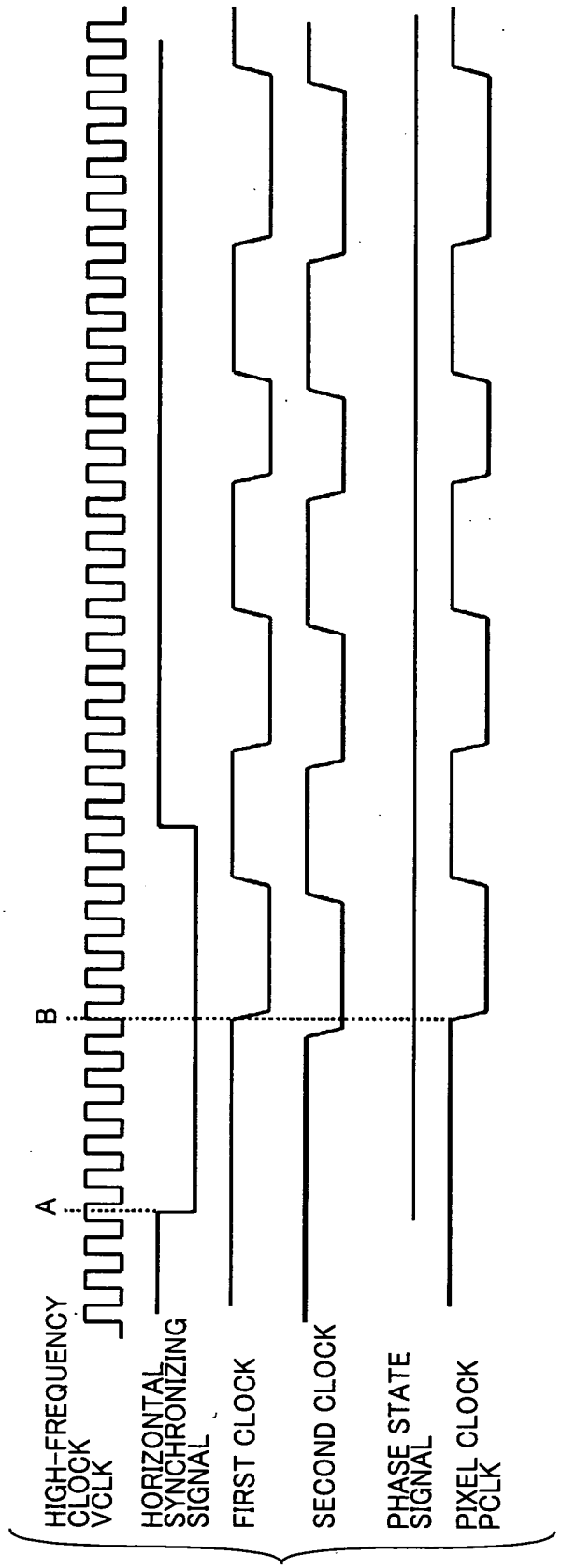

HIGH-FREQUENCY CLOCK VCLK
A
B
HORIZONTAL SYNCHRONIZING SIGNAL
FIRST CLOCK
SECOND CLOCK
PHASE STATE SIGNAL
PIXEL CLOCK PCLK

FIG.17

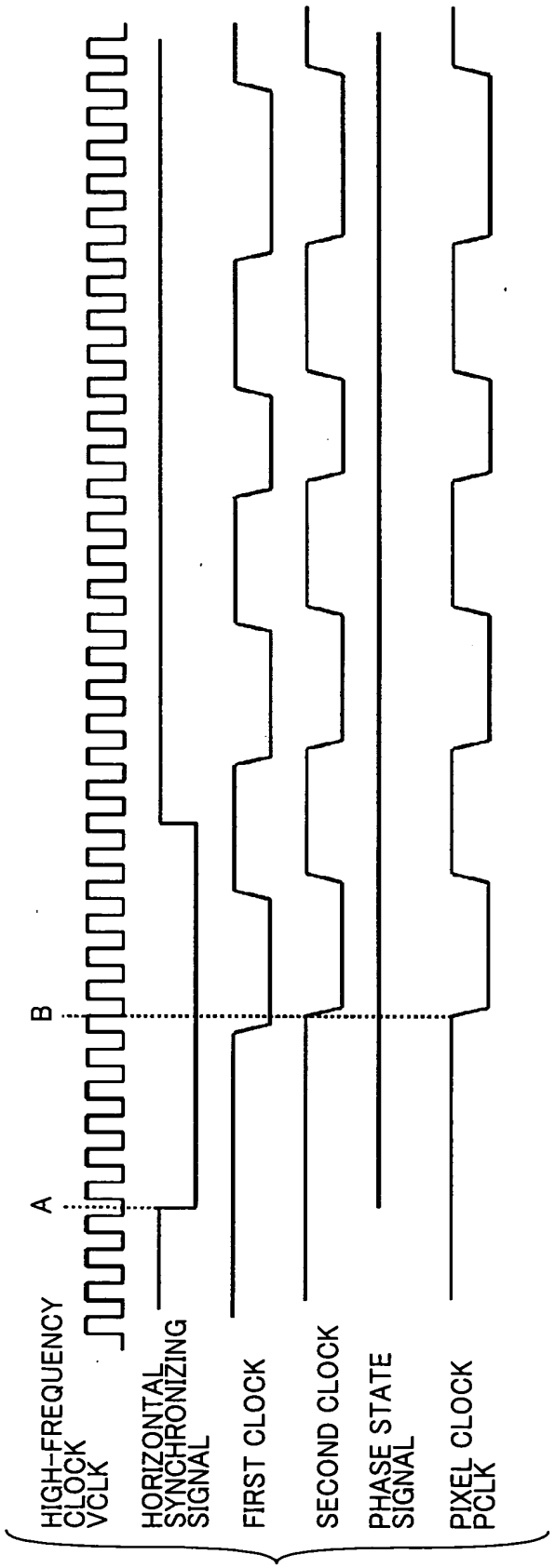

HIGH-FREQUENCY CLOCK VCLK
HORIZONTAL SYNCHRONIZING SIGNAL
FIRST CLOCK
SECOND CLOCK
PHASE STATE SIGNAL
PIXEL CLOCK PCLK
A
B

FIG.18

FIG.19

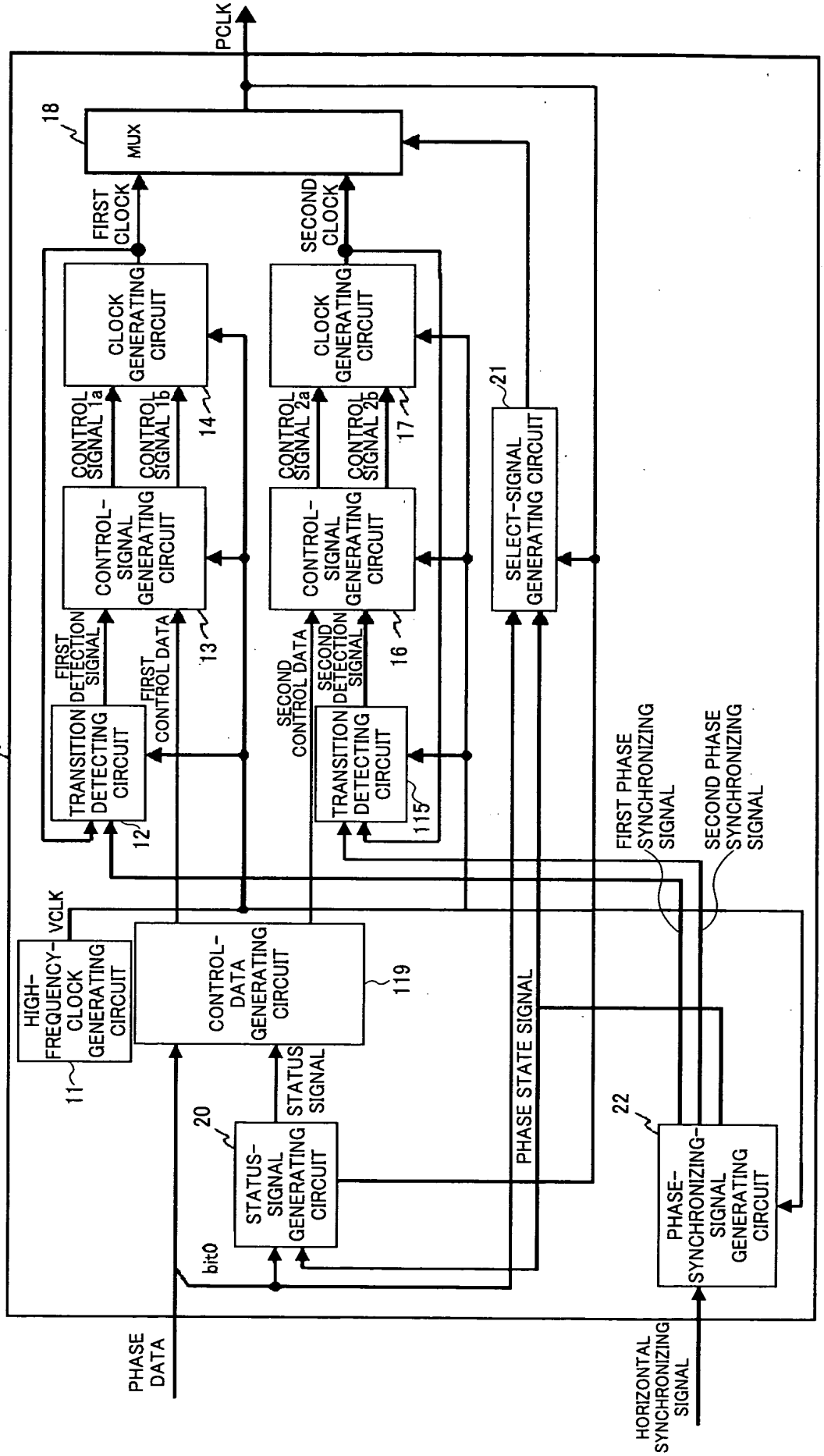

10 PIXEL-CLOCK GENERATING CIRCUIT
PCLK
18
MUX
FIRST CLOCK
SECOND CLOCK
CLOCK GENERATING CIRCUIT
CLOCK GENERATING CIRCUIT
CONTROL SIGNAL 1a
CONTROL SIGNAL 1b
CONTROL SIGNAL 2a
CONTROL SIGNAL 2b
14
17
21
CONTROL-SIGNAL GENERATING CIRCUIT
CONTROL-SIGNAL GENERATING CIRCUIT
SELECT-SIGNAL GENERATING CIRCUIT
FIRST DETECTION SIGNAL
FIRST CONTROL DATA
SECOND CONTROL DATA
SECOND DETECTION SIGNAL
13
16
TRANSITION DETECTING CIRCUIT
TRANSITION DETECTING CIRCUIT
12
115
FIRST PHASE SYNCHRONIZING SIGNAL
SECOND PHASE SYNCHRONIZING SIGNAL
VCLK
HIGH-FREQUENCY-CLOCK GENERATING CIRCUIT
CONTROL-DATA GENERATING CIRCUIT
11
119
STATUS SIGNAL
20
STATUS-SIGNAL GENERATING CIRCUIT
bit0
PHASE STATE SIGNAL
22
PHASE-SYNCHRONIZING-SIGNAL GENERATING CIRCUIT
PHASE DATA
HORIZONTAL SYNCHRONIZING SIGNAL

FIG.20

PHASE SHIFT AMOUNT	PHASE DATA 3bit
0	000
1/16 PCLK ADVANCEMENT	001
2/16 PCLK ADVANCEMENT	010
3/16 PCLK ADVANCEMENT	011
1/16 PCLK DELAY	111
2/16 PCLK DELAY	110
3/16 PCLK DELAY	101

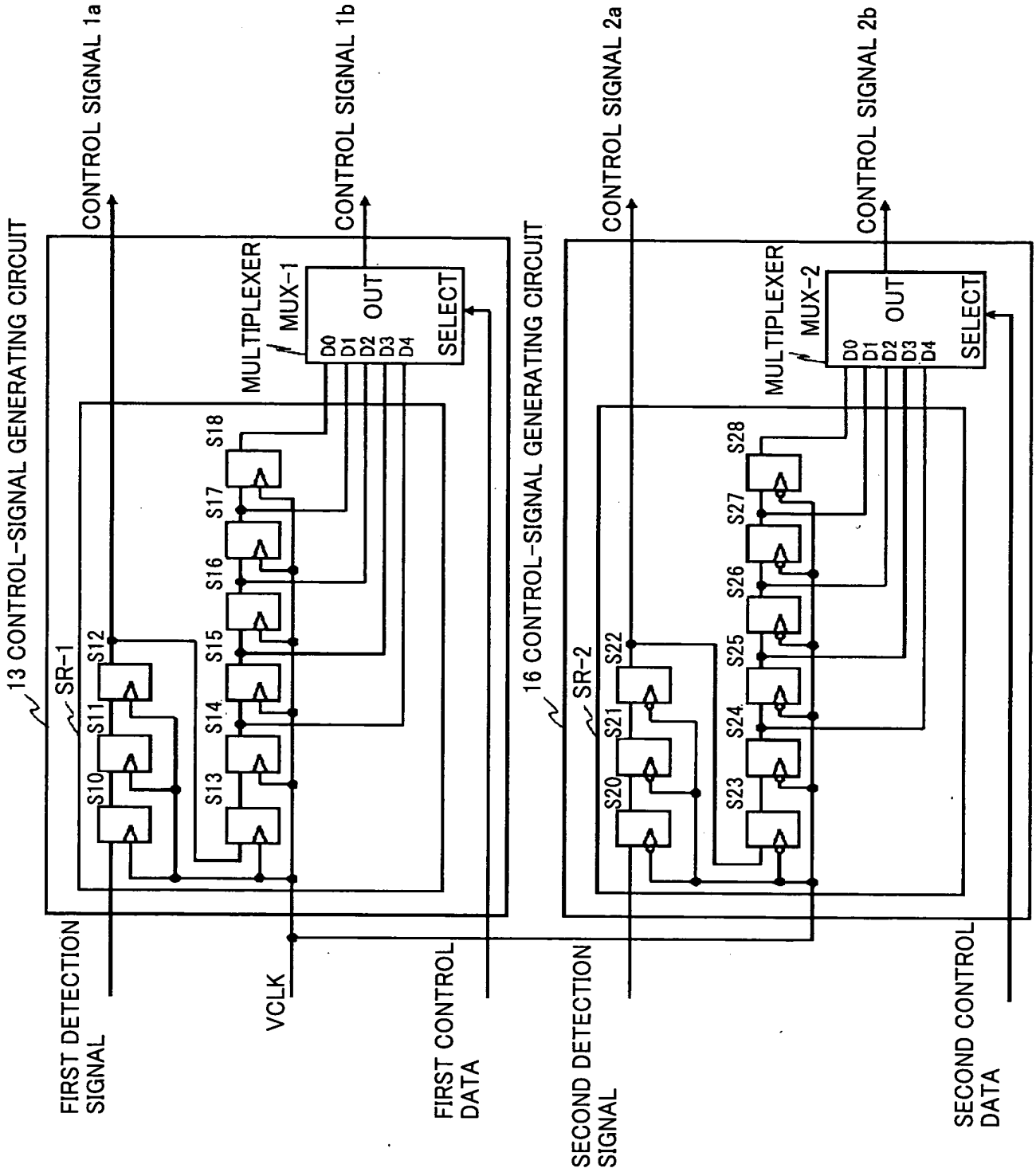

13 CONTROL-SIGNAL GENERATING CIRCUIT
SR-1
S10
S11
S12
S13
S14
S15
S16
S17
S18
MULTIPLEXER
MUX-1
D0
D1
D2
D3
D4
OUT
SELECT
CONTROL SIGNAL 1a
CONTROL SIGNAL 1b
FIRST DETECTION SIGNAL
VCLK
FIRST CONTROL DATA
16 CONTROL-SIGNAL GENERATING CIRCUIT
SR-2
S20
S21
S22
S23
S24
S25
S26
S27
S28
MULTIPLEXER
MUX-2
CONTROL SIGNAL 2a
CONTROL SIGNAL 2b
SECOND DETECTION SIGNAL
SECOND CONTROL DATA

FIG.21

FIG.22

FIRST CONTROL DATA SECOND CONTROL DATA	CONTROL SIGNAL 1b	CONTROL SIGNAL 2b
000	S18	S28
001	S17	S27
010	S16	S26
011	S15	S25
100	S14	S24

FIG.23

PHASE DATA 3bit	STATUS SIGNAL	FIRST CONTROL DATA	SECOND CONTROL DATA
000	0	010	010
000	1	010	010
001	0	010	001
001	1	001	010
010	0	001	001
010	1	001	001
011	0	001	000
011	1	000	001
111	0	011	010
111	1	010	011
110	0	011	011
110	1	011	011
101	0	100	011
101	1	011	100

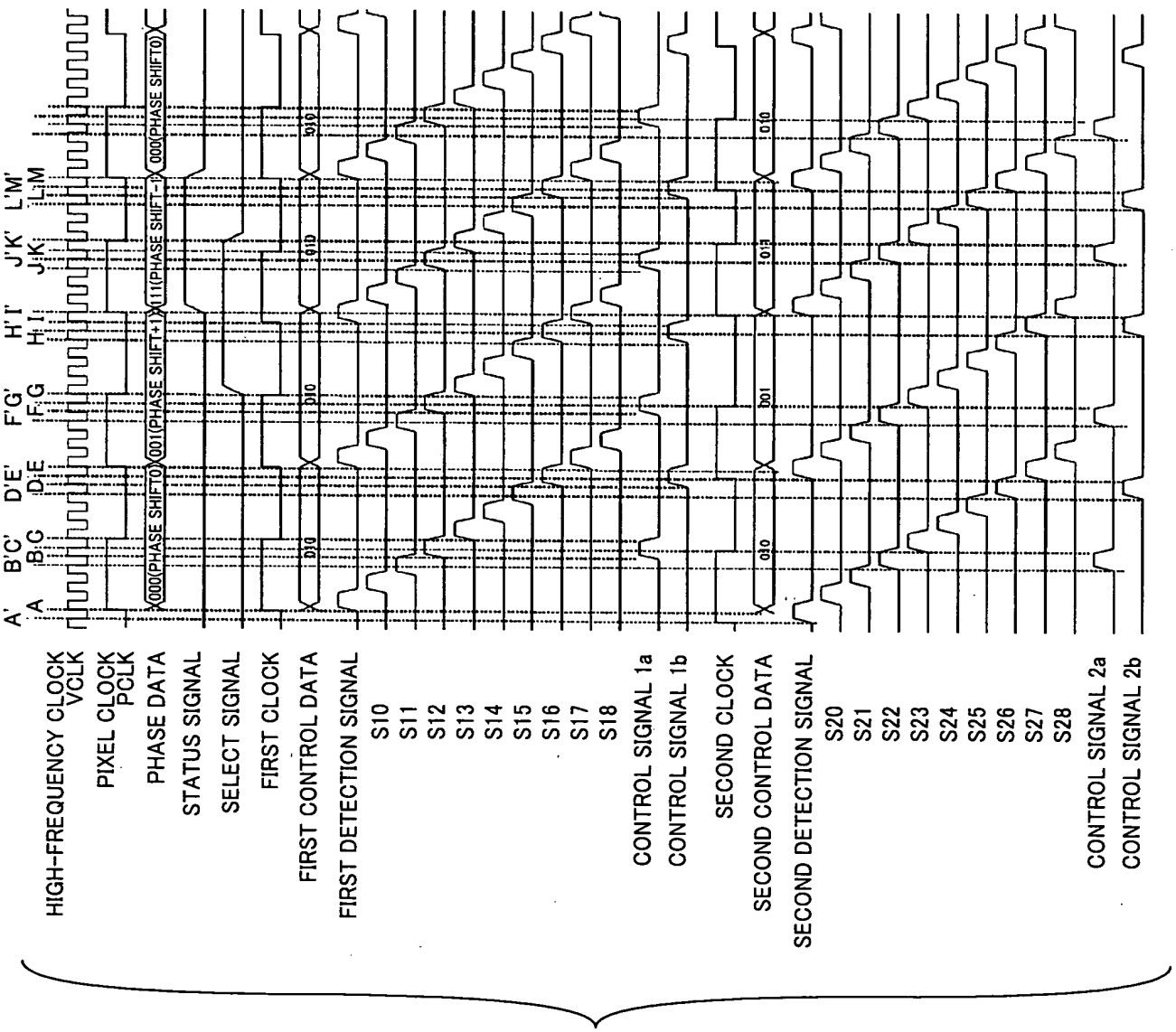

A' A B'C' B C D'E' D E F'G' F G H'I' H I J'K' J K L'M' L M
HIGH-FREQUENCY CLOCK VCLK
PIXEL CLOCK PCLK
PHASE DATA
STATUS SIGNAL
SELECT SIGNAL
FIRST CLOCK
FIRST CONTROL DATA
FIRST DETECTION SIGNAL
S10
S11
S12
S13
S14
S15
S16
S17
S18
CONTROL SIGNAL 1a
CONTROL SIGNAL 1b
SECOND CLOCK
SECOND CONTROL DATA
SECOND DETECTION SIGNAL
S20
S21
S22
S23
S24
S25
S26
S27
S28
CONTROL SIGNAL 2a
CONTROL SIGNAL 2b
000(PHASE SHIFT0)
001(PHASE SHIFT+1)
011(PHASE SHIFT-1)
000(PHASE SHIFT0)
D10
D01
D10
D10
D01
D10

FIG.24

FIG.25

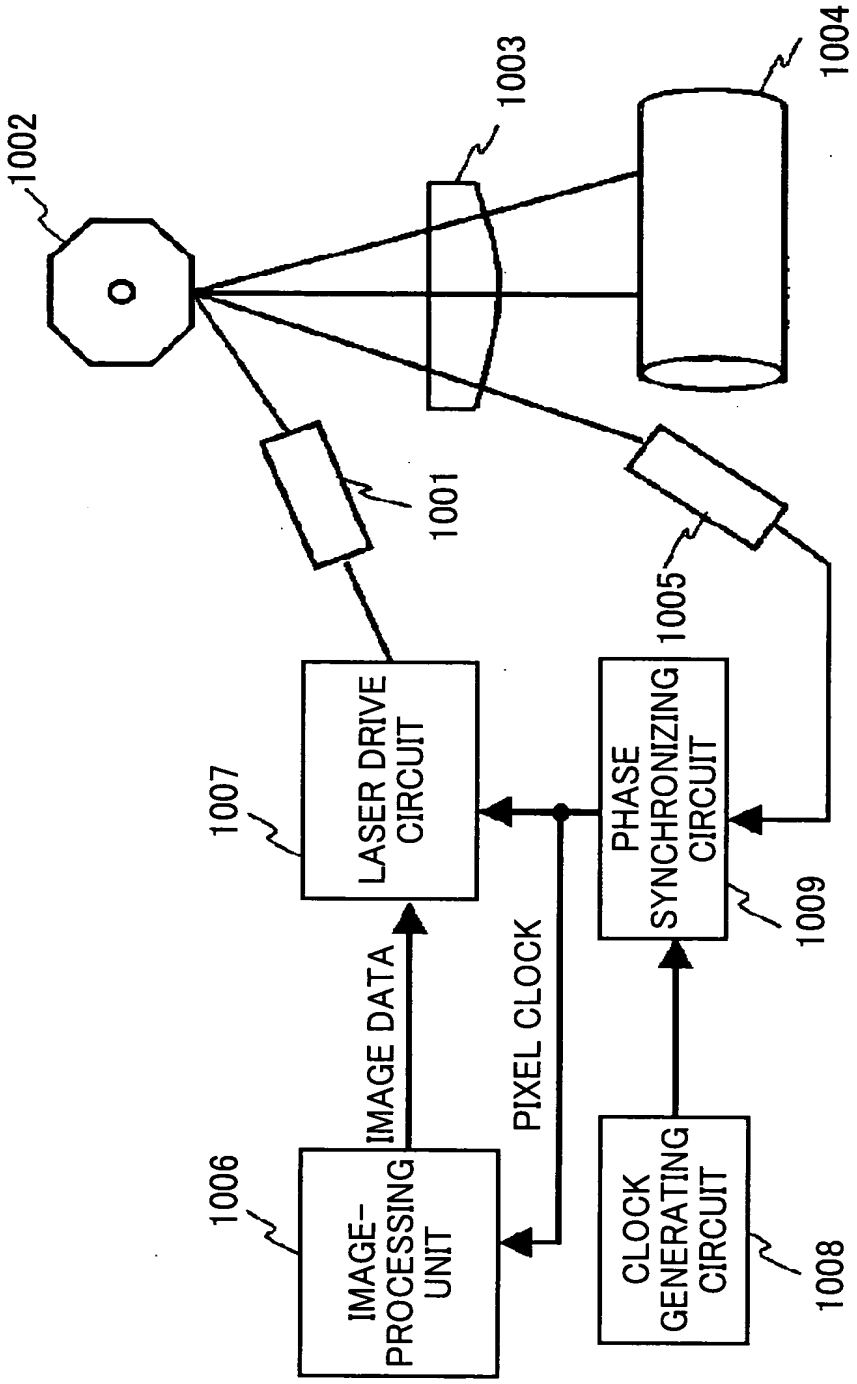

1002
1003
1004
1001
1005
1007
LASER DRIVE CIRCUIT
PHASE SYNCHRONIZING CIRCUIT
1009
IMAGE DATA
PIXEL CLOCK
1006
IMAGE-PROCESSING UNIT
CLOCK GENERATING CIRCUIT
1008

FIG.26

200

	SHIFT AMOUNT
1	0
2	0
3	0
4	−1
5	0
6	0
7	−1
8	0
9	0
10	−1
11	0
12	0
⋮	⋮
2395	0
2396	0
2397	+1
2398	0
2399	0
2400	+1
2401	0
2402	0
2403	+1
2404	0
2405	0
⋮	⋮
4789	0
4790	0
4791	−1
4792	0
4793	0
4794	−1
4795	0
4796	0
4797	−1
4798	0
4799	0
4800	0

+

201

	SHIFT AMOUNT
1	0
2	0
3	0
4	0
5	0
6	0
7	0
8	0
9	0
10	+1
11	0
12	0
⋮	⋮
2395	0
2396	0
2397	0
2398	0
2399	0
2400	+1
2401	0
2402	0
2403	0
2404	0
2405	0
⋮	⋮
4789	0
4790	+1
4791	0
4792	0
4793	0
4794	0
4795	0
4796	0
4797	0
4798	0
4799	0
4800	+1

=

202

	SHIFT AMOUNT
1	0
2	0
3	0
4	−1
5	0
6	0
7	−1
8	0
9	0
10	0
11	0
12	0
⋮	⋮
2395	0
2396	0
2397	+1
2398	0
2399	0
2400	+2
2401	0
2402	0
2403	+1
2404	0
2405	0
⋮	⋮
4789	0
4790	+1
4791	−1
4792	0
4793	0
4794	−1
4795	0
4796	0
4797	−1
4798	0
4799	0
4800	+1